CLAIMS

1. A semiconductor device comprising:

a MIS type field effect transistor which comprises a semiconductor raised portion protruding from a substrate plane, a gate electrode extending over the semiconductor raised portion from the top onto the opposite side faces of the semiconductor raised portion, a gate insulation film existing between the gate electrode and the semiconductor raised portion, and source and drain regions provided in the semiconductor raised portion;

an interlayer insulating film provided on a substrate including the transistor; and

a buried conductor interconnect that is formed by filling in a trench formed in the interlayer insulating film with a conductor,

wherein the buried conductor interconnect connects one of the source and drain regions of the semiconductor raised portion and another conductive portion below the interlayer insulating film.

2. The semiconductor device according to claim 1, wherein the buried conductor interconnect is connected to one of the source and drain regions of the semiconductor raised portion and another conductive portion below the interlayer insulating film, and has an upper face coplanar with the upper face of the interlayer insulating film and a lower face below the upper face of the semiconductor raised portion at an area of connection with the one of source and drain regions.

3. The semiconductor device according to claim 1 or 2, wherein the buried conductor interconnect is in contact with opposite side faces of the

semiconductor raised portion at an area of connection with the one of source and drain regions.

4. The semiconductor device according to claim 1, 2 or 3, wherein the semiconductor device comprises a first transistor and a second transistor as the MIS type field effect transistor, and the buried conductor interconnect is connected to one of source and drain regions of the first transistor and a gate electrode or one of source and drain regions of the second transistor as the another conductive portion.

5. The semiconductor device according to any one of claims 1 to 4, wherein the semiconductor device comprises, as the MIS type field effect transistor, a transistor comprising a plurality of semiconductor raised portions protruding from a substrate plane, a gate electrode formed of a conductor provided over the plurality of semiconductor raised portions and extending from the top to the opposite side faces of each semiconductor raised portion, a gate insulating film existing between the gate electrode and each semiconductor raised portion, and source and drain regions provided in each semiconductor raised portion, and

in the transistor, the buried conductor interconnect is connected to one of source and drain regions of one semiconductor raised portion and one of source and drain regions of another semiconductor raised portion as the another conductive portion.

6. The semiconductor device according to claim 5, wherein the plurality of semiconductor raised portions are arranged mutually in parallel.

7. The semiconductor device according to any one of claims 1 to 6, wherein the buried conductor interconnect is connected through a plug or directly to the upper interconnect.

8. The semiconductor device according to any one of claims 1 to 7, wherein the buried conductor interconnect and one of the source and drain regions are connected through a resistance lowering layer made of a metal or a metallic compound.

9. The semiconductor device according to any one of claims 1 to 8, wherein the semiconductor raised portion has a part where width W of the part along a direction parallel to the substrate plane and vertical to the channel length direction is larger than width W of a part below the gate electrode at least at an area of connection between one of the source and drain regions of the semiconductor raised portion and the buried conductor interconnect.

10. The semiconductor device according to any one of claims 1 to 9, wherein the semiconductor device comprises, as the MIS type field effect transistor, a first conductivity type transistor and a second conductivity type transistor that constitute a CMOS inverter,

gate electrodes of the first conductivity type transistor and the second conductivity type transistor are formed of a common conductor, and the conductor is connected to an input node, and

the buried conductor interconnect is connected to a drain region of the

first conductivity type transistor and a drain region of the second conductivity type transistor, and is connected to an output node.

11. A semiconductor device comprising a SRAM cell unit having a pair of first and second drive transistors, a pair of first and second load transistors and a pair of first and second transfer transistors, wherein

each of the transistors comprises a semiconductor raised portion protruding from a substrate plane, a gate electrode extending over the semiconductor raised portion from the top onto the opposite side faces of the semiconductor raised portion, a gate insulating film existing between the gate electrode and the semiconductor raised portion, and source and drain regions provided in the semiconductor raised portion;

the semiconductor raised portions of the transistors are arranged with their longitudinal direction extending along a first direction;

the first drive transistor and the first transfer transistor have a common first semiconductor raised portion, the second drive transistor and the second transfer transistor have a common second semiconductor raised portion, the first load transistor has a third semiconductor raised portion adjacent to the first semiconductor raised portion, and the second load transistor has a fourth semiconductor raised portion adjacent to the second semiconductor raised portion; and

the gate electrodes of the first drive transistor and the first load transistor are formed of a common first conductor, the gate electrodes of the second drive transistor and the second load transistor are formed of a common second conductor, and the conductors are arranged with their longitudinal direction extending along a second direction vertical to the first

direction.

12. The semiconductor device according to claim 11, comprising:

an interlayer insulating film provided on a substrate including the SRAM cell unit;

a first buried conductor interconnect connected to the first conductor, the drain region of the second load transistor, the drain region of the second drive transistor and one of the source and drain regions of the second transfer transistor, and formed on the interlayer insulating film; and

a second buried conductor interconnect connected to the second conductor, the drain region of the first load transistor, the drain region of the first drive transistor and one of the source and drain regions of the first transfer transistor, and formed on the interlayer insulating film.

13. The semiconductor device according to claim 12, wherein each of the first and second buried conductor interconnects has an upper face coplanar with the upper face of the interlayer insulating film and a lower face below the upper face of the semiconductor raised portion at areas of connection with the source regions and the one of source and drain regions.

14. The semiconductor device according to claim 12 or 13, wherein the first and second buried conductor interconnects are in contact with opposite side faces of the semiconductor raised portions at areas of connection with the source region and the one of source and drain regions.

15. The semiconductor device according to any one of claims 11 to 14

comprising, as the transistor, a transistor comprising a plurality of semiconductor raised portions protruding from a substrate plane, a gate electrode formed of a conductor provided over the plurality of semiconductor raised portions and extending the top to the opposite side faces of each semiconductor raised portion, a gate insulating film existing between the gate electrode and each semiconductor raised portion, and source and drain regions provided in each semiconductor raised portion.

16. A method for producing a semiconductor device comprising a MIS type field effect transistor which comprises a semiconductor raised portion protruding from a substrate plane, a gate electrode extending over the semiconductor raised portion from the top onto the opposite side faces of the semiconductor raised portion, a gate insulating film existing between the gate electrode and the semiconductor raised portion, and source and drain regions provided in the semiconductor raised portion, the method comprising the steps of:

forming the MIS type field effect transistor;

forming an interlayer insulating film so as to bury the semiconductor raised portion;

forming a trench in the interlayer insulating film so as to expose at least a part of one of the source and drain regions provided in the semiconductor raised portion and another conductive portion to be conducted to the one of source and drain regions in the trench; and

filling in the trench with a conductor to form a buried conductor interconnect that is connected to the one of source and drain regions and the another conductive portion.

17. The method for producing a semiconductor device according to claim 16, wherein the another conductive portion is a gate electrode or one of source and drain regions of another transistor.

18. The method for producing a semiconductor device according to claim 16 or 17, wherein

the MIS type field effect transistor comprises a plurality of semiconductor raised portions protruding from a substrate surface, a gate electrode formed of a conductor provided over the plurality of semiconductor raised portions and extending from the top to the opposite side faces of each semiconductor raised portion, a gate insulating film existing between the gate electrode and each semiconductor raised portion, and source and drain regions provided in each semiconductor raised portion, and

in the step of forming a trench, at least a part of each one of the source and drain regions provided in the semiconductor raised portions to be mutually conducted is exposed, and a conductor is filled in the trench to form a buried conductor interconnect that is connected to one of source and drain regions of one semiconductor raised portion and one of source and drain regions of another semiconductor raised portion in the transistor.

19. The method for producing a semiconductor device according to claim 16, 17 or 18, comprising a step of epitaxially growing Si on the surface of the semiconductor raised portion before forming the interlayer insulating film.

20. The method for producing a semiconductor device according to any

one of claims 16 to 19, comprising a step of forming a resistance lowering layer made of a metal or a metallic compound on the semiconductor raised portion before forming the interlayer insulating film.

21. The method for producing a semiconductor device according to claim 16, 17 or 18, comprising a step of epitaxially growing Si on the surface of the semiconductor raised portion exposed in the trench after forming the trench.

22. The method for producing a semiconductor device according to any one of claims 16 to 19 and 21, comprising a step of forming a resistance lowering layer made of a metal or a metallic compound on the semiconductor raised portion exposed in the trench after forming the trench.